Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 11, with the following amended paragraph:

The flexibility of this architecture lies within the connection cell 11 and the switch cell 12. In common terminology, a fully "populated" connection cell 11 will connect each pin of the logic cell ~~12~~ 10 to every wire connecting to the switch cell 12. A "depopulated" connection cell 11 will connect each pin of the logic cell to a subset of the wires connecting to the switch cell 12, with each pin connecting to a different, possibly overlapping, subset of wires. Similarly, a fully "populated" switch cell will provide full crossbar connections between all the wires on all four of its sides, and a "depopulated" switch cell will only provide a subset of these connections. Lastly, the set of wires between any two cells is called a "channel", and the number of wires in a channel can be varied.

Please replace the paragraph beginning at page 9, line 4, with the following amended paragraph:

These 2X2 switches are connected in a specific topology to build a Benes network. For the purpose of illustration, the arrangement of the 2X2 switches 20 in an 8X8 Benes network is shown in Fig. 3A. For a network with N inputs and N outputs, N being a power of 2, there are (2 * ($\log_2$N) – 1) levels of switches, each level consisting of N/2 switches. In this example of an 8X8 network, each level has 4 switch cells and there are 5 levels. The interconnection between the switches 20 can best be understood by viewing the network in a hierarchical arrangement, starting from the outside and proceeding inwards. We can view the two outermost levels, levels 1 and 5, in detail and view the inner levels as hierarchical blocks, as illustrated by Fig. 3B.[[.]] The inner levels can be viewed as two hierarchical blocks, an Upper Network 25 and a Lower Network 26. In level 1, each switch cell 20 has one output going to the Upper Network 25, and one output going to the Lower Network 26. Similarly in level 5, each switch cell has one input from the Upper Network 25, and one input coming from the Lower Network 26.